IN THE SPECIFICATION:

Please revise the specification as follows:

Rewrite the text on pages 5 and 6 of the specification as follows:

SUMMARY OF THE INVENTION

~~The present invention provides a system and method for properly aligning multiple clock domains within a bus system. Variable delays introduced by individual bus system circuits and components operating over a range of conditions can be effectively tracked and removed as skewing inter-clock domain influences. As a result, timing margins are preserved within the bus system.~~

~~In one aspect, the present invention provides a~~ A method of aligning clock signals in a ~~bus~~ system ~~by~~ includes generating a transmit clock signal in a master, and arbitrarily adjusting the phase of the transmit clock signal while maintaining a ~~fixed~~ a first predefined phase relationship between the transmit clock signal and a second system clock. ~~In a related aspect, the present invention provides for~~ A further adjustment of the phase of the transmit clock signal may be made to have a ~~fixed~~ a second predefined phase relationship with a receive clock signal while maintaining the ~~fixed~~ first predefined phase relationship between the transmit clock signal and the second system clock. In one embodiment, ~~this fixed~~ the second predefined phase relationship between the transmit clock signal and the receive clock signal is 180°.

In another aspect, ~~the present invention provides~~ a method of aligning clock signals in a bus system ~~by~~ includes generating a transmit clock signal in a master in relation to a first system clock, shifting the transmit clock signal phase by 90°, and passing the phase shifted transmit clock signal through an output driver circuit in the master to generate a second system clock. As a result and in contrast to the conventional expectation, the first and second system clocks need not be phase aligned.

~~In yet another aspect, the present invention provides a method of aligning system clocks in a bus system by generating a first system clock external to the master such that the first system clock propagates via the channel through the one or more slave towards the master, and generating in the master a second system clock having a phase relation to the first~~

~~system clock defined such that, the phase difference between the first system clock and the second system clock is substantially equal to 90° minus the sum of the receiver setup delay and the output driver delay.~~

~~In another aspect, the present invention provides an identical apparent delay for data traversing a bus system despite voltage and temperature induced variances in the fractional delay and/or cycle delay inherent in the transmission of data to different points within the bus system.~~

~~In still another aspect, the present invention provides a circuit for defining a second system clock in a bus system comprising a master connected to one or more slave devices via a channel, the channel communicating an externally generated first system clock towards the master, the circuit comprising; a delay locked loop circuit receiving the first system clock and a phase feedback signal as inputs and generating a transmit clock signal, a 90° block receiving the transmit system clock and generating a 90° phased shifted version of the transmit clock signal, and an output driver circuit receiving the 90° phased shifted version of the transmit clock signal and generating the second system clock.~~